REMARKS

The Applicant would first like to note that the cover sheet of the pending Office Action appears to include a typographical error in the indicated date mailed. The Office Action indicates that the pending Office Action was mailed March 10, 2005, however according to PAIR the Office Action was instead mailed October 18, 2005.

In the Office Action, the Examiner has rejected claims 1-12, 14-18, and 20-28 under 35 U.S.C. § 103(a) as being unpatentable over Okumura (U.S. Patent No. 4,935,380) in further view of the admitted prior art (APA) and Yoo (U.S. Patent No. 5,605,854). The Examiner correctly notes that Okumura discloses the limitations of forming a gate stack on a substrate, the gate stack having at least one conductive layer of tungsten silicide and a source layer of polysilicon positioned on top of the at least one conductive layer and at an uppermost surface of the gate stack, the source layer capable of providing a source of transforming atoms (silicon).

The Examiner notes that Okumura fails to disclose the limitations of exhuming a first layer of the gate stack so as to expose a portion of the source layer above at least a portion of the gate stack so as to define a first circuit load, comprising removing a portion of a cap insulating layer, depositing a refractory material of titanium so that the refractory material contacts the exposed uppermost portion of the source layer of the gate stack and so that the refractory material is also positioned to contact a second circuit node of the integrated circuit having a rich source of the transforming atoms (silicon), forming a masking layer over the refractory material, etching the masking layer so as to define an extent of a local interconnect, and selectively transforming the refractory material underneath the etched masking layer including at the exposed portion of the source layer and the second circuit node into low resistance contacts wherein the source layer provides transforming atoms to the portion of the refractory material positioned adjacent the exposed upper most portion of the source layer than the second circuit node.

The Examiner further notes that Okumura fails to disclose performing a selective removal process which comprises etching the exposed refractory material after annealing the refractory material with etchant (wet) which is selective for nitrides and substantially less reactive with silicides, wherein portions of the refractory material beyond the masking layer are preferentially removed and wherein the transformed refractory material underneath the masking layer is preferentially unresponsive to the selective removal process. The Examiner also notes that

Okumura fails to disclose annealing the refractory material by exposing the refractory material to a rapid thermal processing environment having an N2/NH3 ambient so as to increase the temperature of the refractory material to a value between 600 degrees Celsius and 750 degrees Celsius for a period of time between 10 seconds and 60 seconds, and wherein the source layer provides the transforming atoms to the refractory material during transformation of the refractory material such that the selective removal process reduces undercutting of the low resistance contact at the exposed surface of the source layer.

The Examiner indicates that the APA discloses exhuming a first layer of the gate stack so as to expose an uppermost surface of the gate stack so as to define a first circuit node, depositing a refractory material of titanium on the integrated circuit so that the refractory material contact the exposed portion of the uppermost layer of the gate stack and so that the refractory material is positioned on a second circuit node of the integrated circuit having a rich source of transforming atoms. The Examiner further notes that the APA discloses forming a masking layer over the refractory material and etching the masking layer so as to define an extent of the local interconnect.

The Applicant notes that the claims of the subject application are amended by this paper to more clearly identify what the Applicant regards as the invention and more particularly now claim

"A method of forming a local interconnect on a semiconductor integrated circuit, the method comprising:

forming a gate stack on a substrate, the gate stack having at least one conductive layer and a source layer positioned on top of the at least one conductive layer and at an uppermost surface of the gate stack, the source layer providing a rich source of ~~transforming atoms~~ silicon;

exhuming a first layer of the gate stack so as to expose a portion of the source layer above at least a portion of the gate stack so as to define a first circuit node;

depositing a refractory material so that the refractory material contacts the exposed uppermost portion of the source layer of the gate stack and so that the refractory material is also positioned to contact a second circuit node of the integrated circuit having a rich source of the ~~transforming atoms~~ silicon;

forming a masking layer over the refractory material;

etching the masking layer so as to define an extent of the local interconnect; ~~and~~

selectively transforming the refractory material in a nitrogen containing ambient such that the refractory material underneath the etched masking layer and at least adjacent the exposed portion of the source layer and the second circuit node is transformed into low resistance contacts comprising ~~the~~ refractory material silicide such that electrical contact between the refractory metal and the at least one conductive level occurs through the source ~~level~~ layer and wherein the source layer provides ~~transforming atoms~~ silicon to the portion of the refractory material positioned adjacent the exposed uppermost portion of the source layer and wherein the refractory material beyond the extent of the local interconnect is transformed to comprise refractory material nitride; and

performing a selective removal process such that the refractory material nitride and remaining refractory material beyond the extent of the local interconnect is preferentially removed and wherein the contacts comprising refractory material silicide are preferentially unresponsive to the selective removal process. (Claim 1 as currently amended, similar additional limitations made by this paper to claim 20).

The Applicant respectfully notes that neither Okumura nor the APA disclose "...selectively transforming the refractory material in a nitrogen containing ambient such that the refractory material underneath the etched masking layer and at least adjacent the exposed portion of the source layer and the second circuit node is transformed into low resistance contacts comprising ~~the~~ refractory material silicide such that electrical contact between the refractory metal and the at least one conductive level occurs through the source ~~level~~ layer and wherein the source layer provides ~~transforming atoms~~ silicon to the portion of the refractory material positioned adjacent the exposed uppermost portion of the source layer and wherein the refractory material beyond the extent of the local interconnect is transformed to comprise refractory material nitride; and

performing a selective removal process such that the refractory material nitride and remaining refractory material beyond the extent of the local interconnect is preferentially removed and wherein the contacts comprising refractory material silicide are preferentially unresponsive to the selective removal process." (Claim 1 as currently amended)

The Applicant respectfully reminds the Examiner that the significant advantage provided by the Applicant's invention of reducing undercutting at the contacts between the local interconnect and the gate stack is facilitated by the selective transformation of the refractory material with a rich source of silicon to form the refractory silicides of the claimed invention. However, a further advantage is provided by the selective transformation of the refractory material in a nitrogen containing ambient which facilitates the use of the selective removal process which in one embodiment is a wet etch to accommodate forming the semiconductor device with small device features.

The Applicant strongly believes that the claimed combination of features is not taught by either of the Okumura, the APA, or the Yoo references. The Applicant further believes that this combination of claimed features would not be obvious to one of ordinary skill and thus believes that the claims as currently amended are patentable under the requirement of 35 U.S.C. § 103(a) over the combined teachings of the art of record, including the Okumura, APA, and Yoo references.

SUMMARY

From the forgoing, the Applicant believes that the subject application as currently amended is allowable over the art of record and respectfully request prompt issuance of a Notice of Allowability. The Applicant notes that this response to a Final Office Action is being filed within two months from the indicated mailing date of the Final Office Action according to PAIR records and respectfully requests that should the Examiner feel that the response does not place the application is a condition for allowance, the Examiner provide an advisory action indicating the reasons therefore. The Applicants further note that while they believe this paper is fully responsive to the rejections made by the Examiner in the Office Action, should there remain any further impediments to the allowance of this application that might be resolved by telephone conference the Examiner is respectfully requested to contact the Applicant's undersigned representative at the indicated telephone number.

Please charge any additional fees, including any fees for additional extension of time, or credit overpayment to Deposit Account No. 11-1410.

Respectfully submitted,

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